CLAIMS

What is claimed is:

1. A cache coherency maintenance system, comprising:

a plurality of cache memories including a cache line for storing information;

a plurality of processor cores included on a single substrate for processing instructions and information stored in said plurality of cache memories wherein one of said plurality of processor cores is coupled to and associated with one of said plurality of cache memories; and

a coherency system bus for communicating information between said plurality of cache memories and said plurality of processor cores in accordance with a coherency protocol, wherein said coherency protocol associates a pending state with said cache line.

2. A cache coherency system of Claim 1 wherein said pending state locks out access to said cache line when said cache line is in transition and continues to lock out access to said cache line until appropriate responses are received indicating continuation of a cache line transaction will not result in race conditions that cause information coherency problems.

3. A cache coherency system of Claim 1 wherein said pending state is one of a plurality of states comprising a pending invalidate write miss state, pending copy back state, and pending copy forward state.

4. A cache coherency system of Claim 3 wherein said pending invalidate write miss state is a state in which a cache line transaction is waiting for invalidate acknowledgments from other caching agents on said system bus and when said invalidate acknowledgments are received, the pending invalidate write miss state transitions over to a modified state that permits a write operation to proceed.

5. A cache coherency system of Claim 3 wherein said pending copy back state is a state in which a cache line transaction is waiting for a copy back reply message and said cache line enters said pending copy back state during a write back due to an external write miss.

6. A cache coherency system of Claim 3 wherein said pending copy forward state is a state in which a cache line transaction is waiting for a copy forward reply message and said cache line enters said pending copy forward state during a cache to cache transfer due to an external read miss.

7. A cache coherency system of Claim 3 wherein said pending states lock out access to a cache line that is in transition between primary states thereby ensuring coherency and preventing race conditions from developing during the completion of a cache line transaction.

8. A cache coherency system of Claim 7 wherein said bus cache coherency protocol further includes three primary cache line states comprising:

a modified state in which said cache line includes a recent value;

a shared state in which said cache line includes the same value as in another memory; and

an invalid state in which said cache line is not available for access in the particular cache in which it is in the invalid state.

9. A cache coherency system of Claim 8 wherein an internal access to said cache line in said invalid state misses said cache line and causes one of said plurality of processor cores to fetch information associated with said cache line from said system bus.

10. A cache coherency system of Claim 8 wherein said cache line is in said modify state in one of said plurality of caches and in said invalid state in the rest of said plurality of caches.

11. A cache coherency system comprising:

a plurality of cache memories including a cache line for storing information;

a plurality of processor cores on a single substrate for processing instructions and information stored in said plurality of cache memories wherein one of said plurality of processor cores is coupled to and associated with one of said plurality of cache memories; and

a coherency system bus for providing coherency in accordance with a memory coherency maintenance method, wherein said memory coherency maintenance method maintains coherency throughout a shared memory model including said plurality of cache memories.

12. A cache coherency system of Claim 11 wherein said memory coherency maintenance method comprises:

attempting to access information in a first memory;

entering a pending state;

changing to a modify state;

transitioning to an invalid state; and

shifting to a shared state.

13. A cache coherency system of Claim 11 wherein said memory coherency maintenance method comprises a pending state that locks out access to information included in one of said plurality of caches while transitioning between other states.

14. A cache coherency system of Claim 11 wherein one of said plurality of processors attempts to access information from an external cache.

15. A cache coherency system of Claim 11 wherein a modified state is entered in one of said plurality of cache memories and the information is put into an invalid state in the remaining of said plurality of cache memories.

16. A cache coherency system of Claim 11 further comprising an embedded memory for storing information and data for downloading to said plurality of cache memories and utilization by said plurality of processors.

17. A cache coherency system of Claim 16 wherein said cache line is in a shared state and comprises the same value as in said embedded main memory.

18. A cache coherency method comprising:

pausing actions to a cache line;

invalidating said cache line;

modifying said cache line; and

sharing said cache line.

19. A cache coherency method of Claim 18 wherein said sharing a cache line includes a sharing control process further comprises:

permitting internal reading of said cache line without shared bus activity; and

producing a invalid cache line transaction when said cache line is internally written.

20. A cache coherency method of Claim 18 further comprising:

producing an internal access line miss; and

causing a processor core to fetch said cache line information from a on chip system bus (OCSB).

21. A cache coherency method of Claim 18 wherein modifying said cache line produces a modified cache line state and includes a more recent value than a main memory.